Thin-film lateral phase-change memory driven by poly-Si MOS transistor enabling both low cost and high-programming gigabyte-per-second throughput

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Abstract

A phase-change memory (PCM) driven by poly-Si MOS transistors was fabricated. The thin phase-change-material layer deposited directly on the channel silicon layer in the PCM enables low-current reset operation (45 μA) compared to the conventional memory structure. With the aid of this low reset current, this memory-cell configuration enables both a poly-Si MOS-driven stackable memory array and large degree programming parallelization. A contactless simple cell structure makes it possible to reduce the cell size to $4F^2$ and the number of process steps. Low cost and gigabyte-per-second programming throughput are thus made possible by this stackable phase-change memory.

Key words: thin-film phase-change memory, poly-Si MOS, stackable

Introduction

Flash memory and phase-change-memory (PCM) technology have been studied extensively [1–5]. Some of them can be used in fabricating a stacked-layered memory with ultra-high density suitable for solid-state disks or storage-class memory. Recent results including some on planar flash memory [6] are summarized in Table 1. Flash memory realizes high density according to the state-of-the-art “2x nm” design rule, but its high-voltage operation makes it difficult to reduce cell size further. Three-dimensional flash memory, such as BiCS flash [1], faces the same issue. PCM is the most promising candidate because of its low operating voltage, scalability, and high programming speed. However, so far, the large reset current of conventional PCM requires a large selection device such as a transistor or diode on the silicon substrate and thus prevents reduction of PCM cell size. In addition, the large reset current limits the degree of parallelization. In this work, we fabricated a PCM with a poly-Si MOS transistor and a thin-film phase-change layer directly deposited on a channel poly-Si. In this PCM, the sectional area perpendicular to the current path in the phase-change layer can be reduced by decreasing film thickness irrespectively of the photo-lithographic limitation. Reset current was thus reduced. As a result, the PCM can be driven by a poly-Si selection MOS transistor. Since it is not necessary to utilize the selection device on a silicon substrate for each memory cell, the PCM can be stacked to achieve ultra high density. A contactless, simple memory structure enables us to reduce cell size and number of process steps. The low reset current of 45 μA and the reset time of 30 ns can achieve gigabyte-per-second programming throughput.

Table 1. Memory technology

	This work	Ref. [6]	Ref. [1]	Ref. [5]	Ref. [4]
Memory	**PCM**	Flash memory		PCM	
	poly-Si MOS	2D bulk MOS	poly-Si MOS	OTS	Poly-Si diode
Scalability	✓			✓	✓
Reset current	**45 μA**				140 μA
Stackable	✓		✓	✓	✓

Structure and operation

Figure 1 shows the structure and operation principle of the developed PCM. The gate oxide, channel poly-Si, and the phase-change material are deposited on the poly-Si gates. The poly-Si transistors are connected serially. A channel poly-Si layer and a phase-change layer are connected in the lateral direction and separated in the direction perpendicular to Fig. 1. In the set/reset operations, a negative off-voltage is applied to the gate at the selected cell, and a positive on-voltage is applied to the gates at the unselected cells. When the set/reset pulse voltage is applied to the drain, the current flows through the phase-change film at the selected cell, and resistive switching occurs. The results of an electro-thermal simulation of the reset operation are also shown in Fig. 1. The temperature at the phase-change layer at the selected cell is increased by Joule heating; thus, a reset operation is produced. In the same way, by applying a voltage suitable for the reading operation to the drain, the resistance of the phase-change film at the selected cell can be determined.

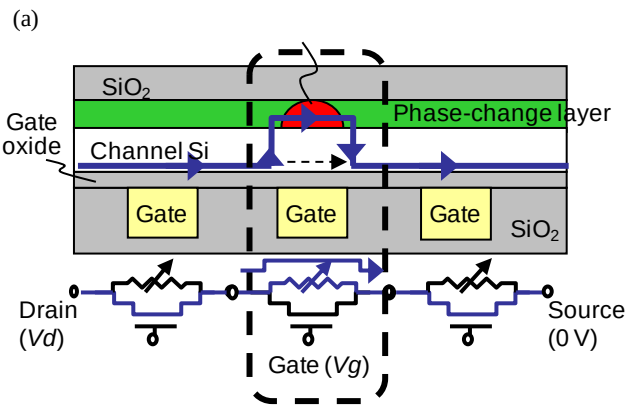

Figure 1. Device structure and operation of the PCM

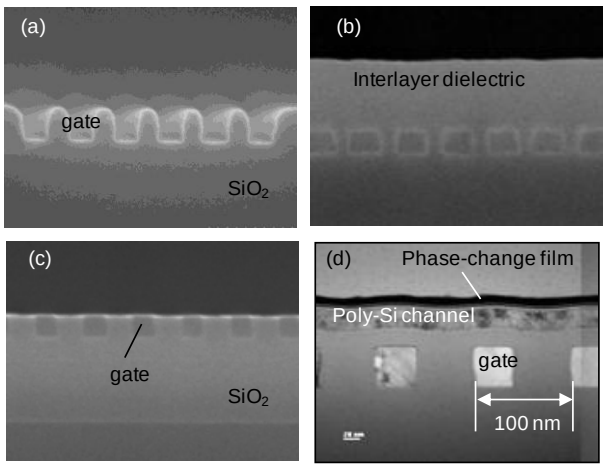

Figure 2. Process flow of lateral PCM array

Fabrication process flow

The fabrication process flow of the memory array is shown in Fig. 2. After a silicon film is deposited on SiO_2 layer, the film is patterned. The stripe line/space pattern of the gate poly-Si is formed as shown in Fig. 2(a). Next, silicon oxide is deposited (Fig. 2(b)) and planarized by CMP (Fig. 2(c)). Next, the gate oxide and channel silicon layers were deposited. A thin film of phase-change material is then deposited on the channel poly-Si. Because a low-thermal-budget process is used for poly-Si MOS, the thermal budget for the crystallization and dopant activation of poly-Si does not affect the phase-change film in a stacking memory array. The channel poly-Si and phase-change material are patterned and, finally, the contacts for the gates and source/drain at both sides of the lateral serial cells are formed (Fig. 2(d)).

Poly-Si MOS transistor

On-current of the poly-Si MOS transistor is significantly affected by the unevenness of the gate oxide/channel interface. The simulated results for on-current are shown in Fig. 3. The recess of the gate or interlayer dielectric should be less than 5 nm, which was achieved in the device, as shown in Fig. 2. The on-current is also strongly dependent on gate-space distance. Figure 4 shows gate-space-distance dependence of the on-current of the poly-Si MOS. The on-current increases with design-rule scaling (i.e., decreasing gate-space distance). According to the specification of the device, gate-space distance should be less than 50 nm.

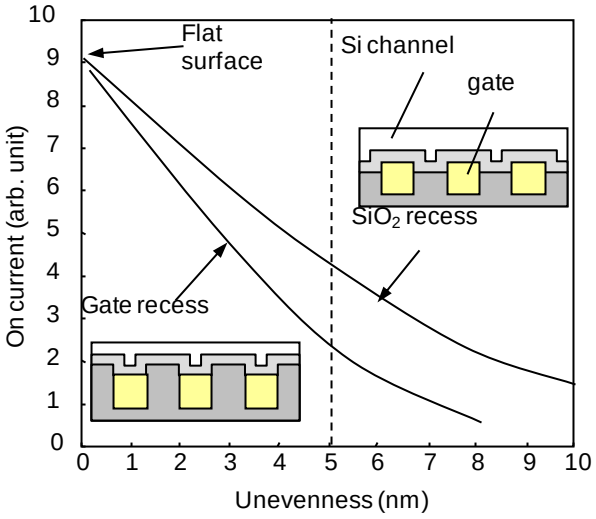

Figure 3. Effect of unevenness on *Ion* of poly-Si MOS transistor

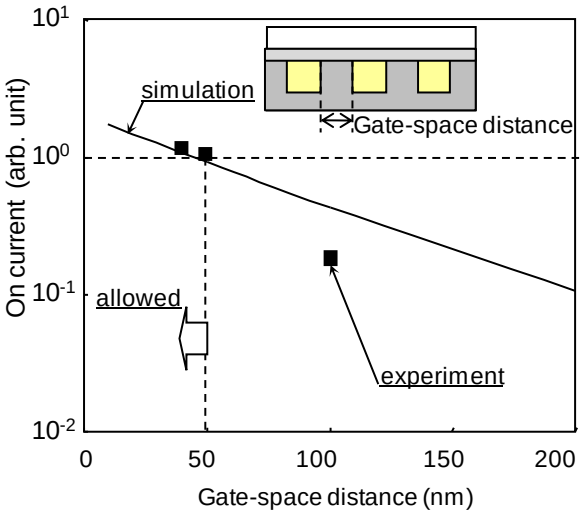

Figure 4. Gate-space dependence of poly-Si-MOS-transistor on current

Characteristics of phase change memory

Figure 5 shows the current-voltage characteristics of the set/reset state of the cell. Each memory cell consists of a parallel connection of the transistor and the phase-change device; therefore, the drain current is the sum of their currents. By applying a negative voltage to the gate, the transistor current is reduced, and the current through the phase-change film is detectable. The resistance ratio between the set and reset states is at least ten. It was found that the high-resistance reset state was switched to low-resistance set state by annealing at 200°C for 3 minutes, indicating that the switching mechanism of the cell is a crystal-amorphous phase change.

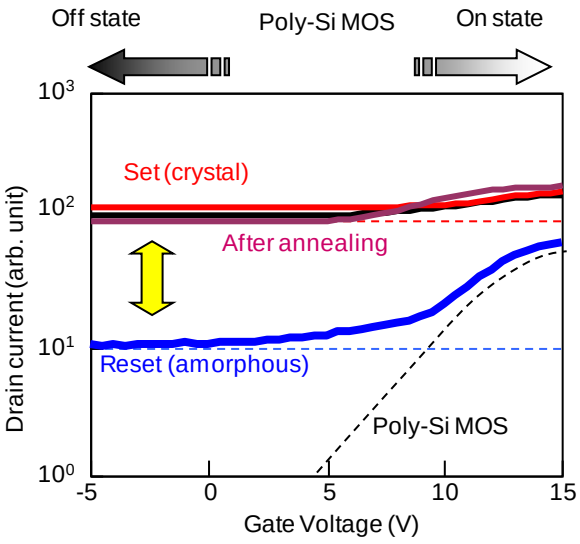

Figure 5. I-V characteristics of the reading operation

The reset current of the device was 45 μA with 30-ns pulse width, as shown in Fig. 6, which is much lower than our previous result (Ref. [4] in Table 1). This low-current reset current is achieved by reducing the cross sectional area of current path with using thin film phase-change layer. Under the assumption that the chip current is 10 mA, this result corresponds to 1-GB/s programming throughput.

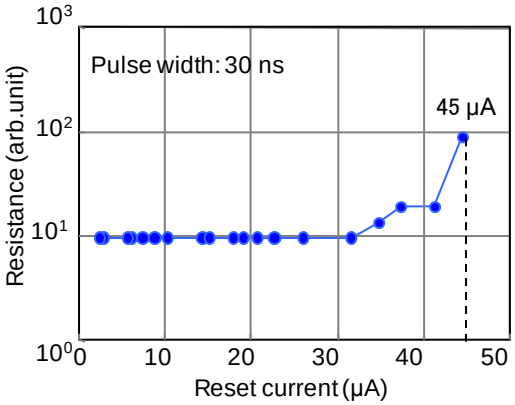

Figure 6. Reset characteristics

Cycle endurance up to 100 times with the resistance ratio of over 10 was confirmed as shown in Fig. 7. The breakdown of the PCM was not observed.

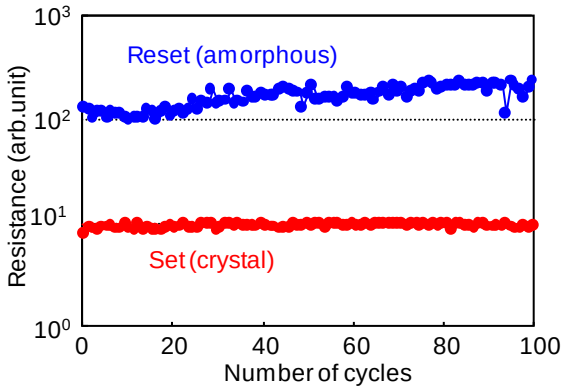

Figure 7. Endurance characteristics

The number of cycles is considered to be affected by the stability of the interface between the phase-change layer and channel silicon layer. Accordingly, we checked the stability at the interface by measuring interdiffusion. We observed no diffusion of silicon or GeSbTe at the interface between the poly-Si channel and GeSbTe after 10-minute annealing at 730℃ as shown in Fig. 8. The temperature of the phase-change layer reaches

the melting point, that is, 630℃, during the reset operation. This result shows that the interface between the silicon and the phase-change layer has enough stability for cycle endurance of over 10^6.

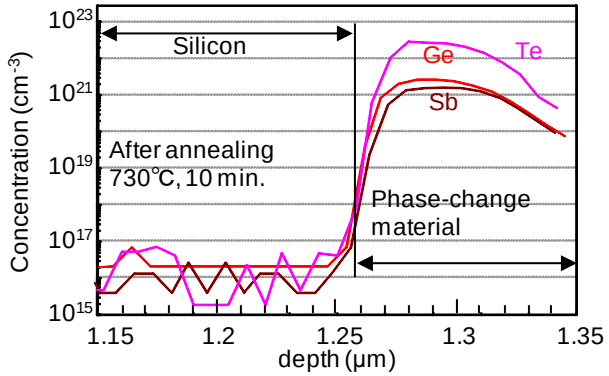

Figure 8. Diffusion of Si and GeSbTe

The retention characteristics of the reset state were also measured as shown in Fig. 9 and are clearly similar to those of conventional PCM devices [2]. We assumed that the retention time is determined by the characteristics of the phase-change material and is independent of the device structure of the memory cell. In other words, the developed cell structure itself does not affect the retention characteristics.

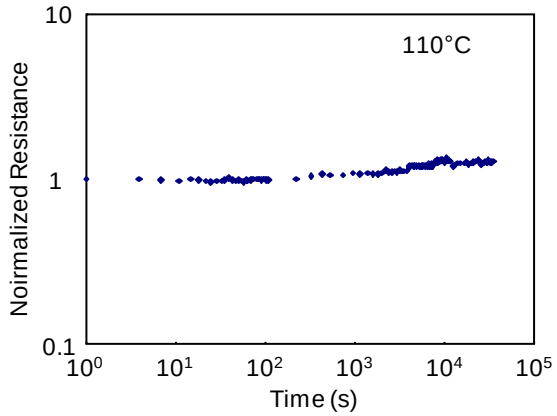

Figure 9. Retention characteristics

The PCM device we developed utilizes a poly-Si MOS transistor, that is, not a silicon substrate device, as a selection device; therefore, stacking of the memory array is possible. Of course, a low-thermal-budget process is necessary for fabricating poly-Si MOS transistor so as not to deteriorate the underlying phase-change layer. The stacking memory array makes it possible to realize an ultra-low-bit-cost PCM device suitable for storage application.

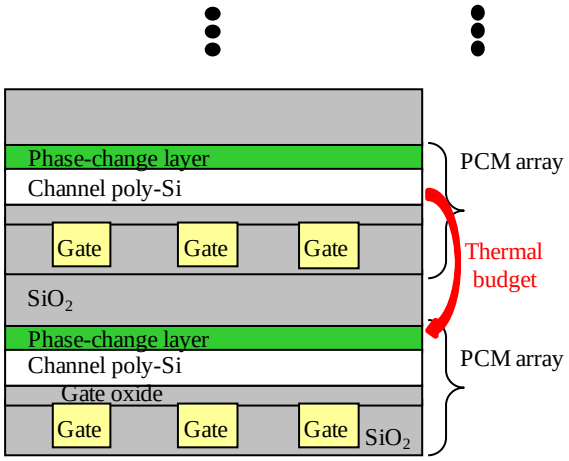

Figure 10. Stacking of PCM array

Summary

A stackable serially connected thin-film lateral-phase-change memory (PCM) with a poly-Si MOS transistor was fabricated. This PCM device achieves both low bit cost and high programming throughput and successfully performs set/reset operation.

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