

Random access multi-levels phase changing using pulse modulation

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ABSTRACT

We describe pulse modulation for random access multi-levels lateral type (ML-) phase change memory (PCM). We have proposed ML-PCM using 2-steps-pulse with various 2nd pulse width like a stair as one of pulse modulations for decreasing and increasing the resistance. We demonstrate that the crystalline region is controlled using the pulse modulation, theoretically and experimentally. Using the stair pulse with 1st pulse with 11 V for 20 ns and 2nd pulse with 4 V for 0 to 400 ns, we could control the resistance of 40k Ω to 600k Ω with random access.

1. INTRODUCTION

Recently, electronic devices require many nonvolatile memories for easy and fast operation of them with small consumptive power. There are many kinds of the nonvolatile memories such as flash memory, magnetic (M-) random access memory (RAM), ferroelectric (Fe-) RAM, phase change (P-) RAM, etc. The PRAM has some advantages. One of them is to operate as multi-levels memory as same as the flash memory. We have already studied the multi-levels phase changing using the current controlling. [1, 2] The method is suitable to change the resistance from high to low value by current controlling. In a case of changing it from low to high value, it is, however, very difficult to increase the resistance by the current controlling.

In order to develop the multi-levels-phase changing with a random access, we have proposed pulse modulation method using 2-steps-pulse control like a staircase. [3] Because the PCM is heated by applying the voltage and current, it is precisely controllable to change the resistance to lower level in the set process, and it is easy to change the phase to complete amorphous state from crystalline state. It is very difficult to change the resistance to higher level reversely. Consequently, our idea reaches to the pulse modulation method that controls the temperature of the PC material to change the phase of partial region to crystalline state by annealing just after the material is completely melt to change to amorphous state. The similar method has been applied to precise writing in digital versatile disk (DVD) optical recording with laser pulse modulation. The plural steps pulse recording has also been introduced in multi-levels PCM by T. Nirschl et al. [4]

In this research, the partial crystallization is achieved by controlling the annealing time in the 2nd pulse. We have studied the possibility to do random access writing in multi-levels PCM using the pulse modulation theoretically and experimentally.

2. SIMULATIONS

The device model was used with lateral type PCM with a top heater as shown in Fig. 1. The simulation executed a way to control the temperature of the PC material, Ge₂Sb₂Te₅ (GST) using 2-steps-pulse as follow. At first, the

temperature increases to higher than melting point by applying the 1st pulse of 11 V for 20 ns. Then, it is kept between crystallizing and melting points by applying the 2nd pulse of 4 V for desired time. Consequently, the resistance is controlled to desired value by applying the 2-steps-pulse between the TiN electrodes. In the simulation, the 2nd pulse duration of from 0 ns to 400 ns was used. Figure 2 shows the 2-steps-pulse and variations of the maximum temperature in the GST layer. The simulated result shows the temperature can be approximately maintained between crystallizing and melting points for the 2nd pulse width.

3. EXPERIMENTS

The prototyped PCM structure was shown in Fig. 3. The top heater was used with TiSiN film with a resistibility of about $5.7 \times 10^{-3} \Omega\text{cm}$ and a thickness of about 80 nm. The resistibility was selected by requirement of minimum application voltage to obtain the critical field of about 38 V/ μm for filament path generation and to directly heat the GST region without heating the heater for reset process. When the 2-steps pulse was applied to the GST under the same condition as the simulation, we could increase the resistance from 40 k Ω to 600 k Ω as shown in Fig. 4. We controlled the resistance by changing the 2nd pulse width of 0 to 400 ns as shown in Fig. 5. This means that the crystalline region increases with the 2nd pulse width gradually after the PC material changed to amorphous region completely. The mechanism of phase change can be considered as shown in Fig. 6 because the annealing was done in the center region of PC material by applying the 2nd pulse.

4. CONCLUSION

We have proposed multi-levels lateral type phase change memory using the 2-steps-pulse modulation like a stair with various 2nd pulse widths. The simulation and experimental results have been obtained as follows.

- (1) The 1st pulse has a role to change the phase to complete amorphous state.
- (2) The 2nd pulse has a role to change a part of the amorphous region to crystalline region.
- (3) The 2nd pulse width controls the resistance to decrease and increase for random access multi-levels recording.
- (4) The resistance changed to 40k Ω to 600k Ω by applying the widths of 400 to 0 ns, respectively.
- (5) The crystalline region is created inside of the amorphous region by the 2nd pulse as shown in Fig. 6.

REFERENCES

1. Y. Yin, T. Noguchi, H. Ohno, and S. Hosaka: "Programming margin enlargement by material engineering for multi-level storage in phase-change memory", *Appl. Phys. Lett.*, **93** (2009) 133503 1-3.
2. Y. Yin, N. Higano, H. Sone, and S. Hosaka: "Ultramultiple-level storage in TiN/SbTeN double-layer cell for high-density non-volatile memory", *Appl. Phys. Lett.*, **92**, (2008) 163509 1-3.
3. S. Hosaka, Tomoyuki Noguchi, and You Yin, "Multi-levels phase change memory using pulse modulation", *EPCOS2010*. (Milano, 2010.9).
4. T. Nirschl et al.: "Write strategies for 2 and 4-bit multi-level phase change memory", *Int. Electron Devices Meet.* (2007) 461-464.

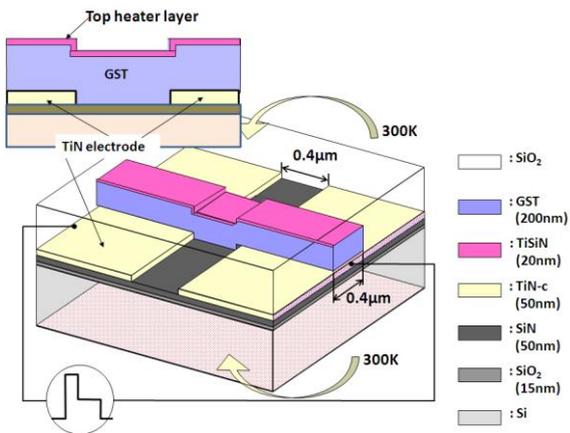


Fig. 1 Simulation model of device structure for FEM method.

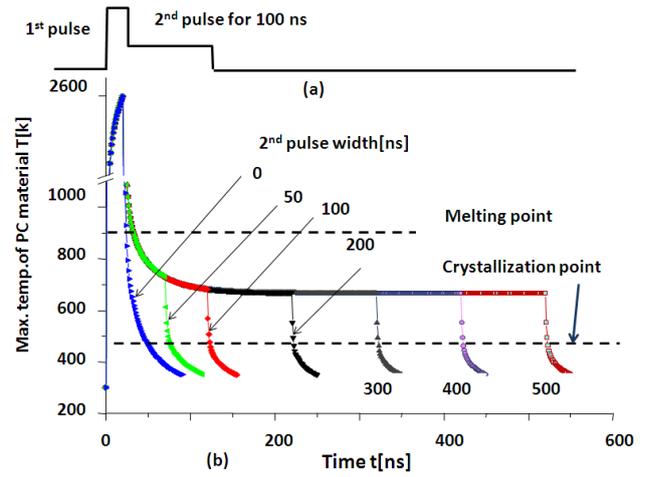


Fig. 2 Simulation results of maximum temperature variations of PC material by 2-steps-pulse like stair, (a) input pulse in a 2nd pulse width of 100 ns, and (b) maximum temperature changes at various 2nd pulse widths.

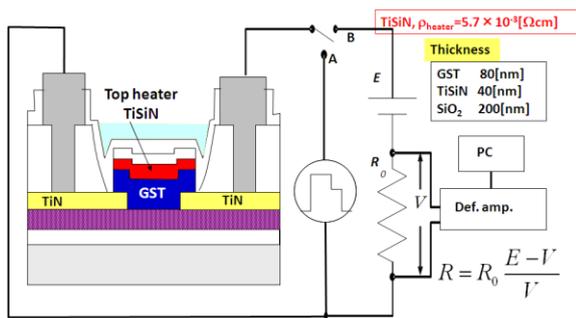


Fig. 3 Device structure of the prototyped lateral type phase change memory (L-PCM) with a top heater

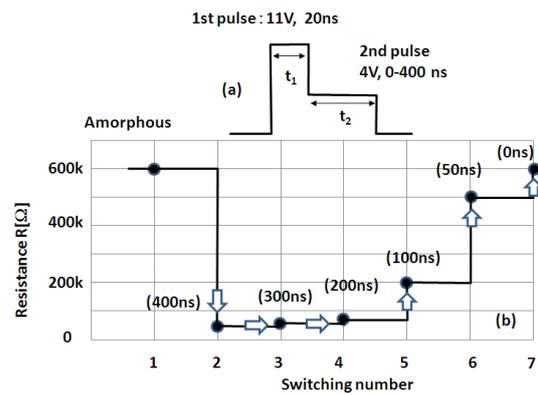


Fig. 4 Variation of the PC resistance by application of 2-steps pulse with various 2nd pulse widths of 0 to 400 ns (the pulse

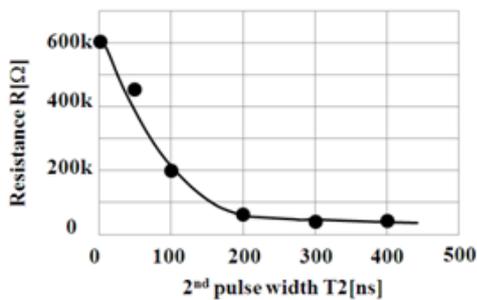


Fig. 5 Variation of PC resistance for 2nd pulse width at 4 V, applying 11 V for 20 ns as 1st pulse.

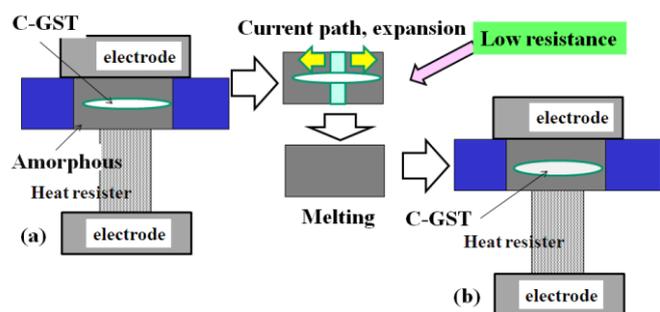


Fig. 6 Phase change flow of the 2-steps-pulse modulation from high to low resistance ((a) to (b)).